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1. Amendments to the Claims:

A listing of the entire set of pending claims (including amendments to the claims, if any) is submitted herewith per 37 CFR 1.121. This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently Amended) Data processing system comprising:

- a clustered Instruction Level Parallelism processor, comprising a plurality of clusters ~~(A—D)~~ each comprising at least one register file and at least one functional unit;
- an instruction unit ~~(IFD)~~ for issuing control signals to said clusters ~~(A—D)~~, wherein said instruction unit ~~(IFD)~~ is connected to each of said clusters ~~(A—D)~~ via respective control connections ~~(CA—CD)~~, and

~~wherein~~ one or more additional pipeline registers ~~(P)~~ is arranged in said control connections ~~(CA—CD)~~ depending on the distance between said instruction unit ~~(IFD)~~ and said clusters ~~(A—D)~~, said pipeline registers being adapted to provide a dedicated direct signal data signal connection between any two of said clusters.

2. (Currently Amended) Data processing system according to claim 1, wherein said clusters ~~(A—D)~~ are connected to each other via a point-to-point connection.

3. (Currently Amended) Data processing system according to claim 1, wherein said clusters ~~(A—D)~~ are connected to each other via a bus connection ~~(100)~~.

4. (Currently Amended) Data processing system according to claim 3, wherein said control connections ~~(CA—CD)~~ are implemented as a bus ~~(110)~~.

5. (Currently Amended) A clustered Instruction Level Parallelism processor, comprising:

- a plurality of clusters ~~(A—D)~~ each comprising at least one register file and at least one functional unit;
- an instruction unit ~~(IFD)~~ for issuing control signals to said clusters ~~(A—D)~~,

wherein said instruction unit ~~(IFD)~~ is connected to each of said clusters ~~(A—D)~~ via respective control connections ~~(CA—CD)~~, and

~~wherein~~ one or more ~~additional~~ additional pipeline register ~~(P)~~ is arranged in said control connections ~~(CA—CD)~~ depending on the distance between said instruction unit ~~(IFD)~~ and clusters ~~(A—D)~~, said pipeline registers being adapted to provide a dedicated direct signal data signal connection between any two of said clusters.

6. (New) The clustered Instruction Level Parallelism processor as claimed in claim 5, wherein said clusters are connected to each other via a point-to-point connection.

7. (New) The clustered Instruction Level Parallelism processor as claimed in claim 5, wherein said clusters are connected to each other via a bus connection.

8. (New) The clustered Instruction Level Parallelism processor as claimed in claim 7, wherein said control connections are implemented as a bus.